AMENDMENTS TO THE CLAIMS

1. (Currently amended) A fixed pixel display device provided with a multiple number M ($M \geq 2$) of stripe-shaped scanning electrodes extending in a first direction and another multiple number N ($N \geq 2$) of stripe-shaped data electrodes extending in a second direction different from said first direction such that light-emitting regions formed of overlap regions of said scanning electrodes and said data electrodes are arrayed in a two-dimensional matrix form of M rows × N columns, wherein:

said fixed pixel display device is provided with actuation drivers connected to the respective data electrodes to actuate said data electrodes;

each said actuation driver ~~drivers each~~ comprises a switching circuit, an output circuit, and a subtraction circuit;

said switching circuit is provided with:

(A) a first switching circuit for applying a first voltage V_1 to the corresponding data electrode,

(B) a second switching circuit for applying a second voltage V_2 ($V_2 \neq V_1$) to the corresponding data electrodes, and

(C) a comparator for performing on/off control of said first switching circuit and second switching circuit;

a voltage, outputted from said output circuit on a basis of a value $D_{m,n}$ (m: any one of 2, 3, ..., M; n: 1, 2, ..., N) of data for controlling states of light emission at a multiple number N of light-emitting regions formed of the scanning electrode in an m^{th} row, is applied for a fixed duration to the data electrode in an n^{th} column; and

a value $(D_{m,n} - D_{m-1,n})$, obtained by subtracting at said subtraction circuit a value $(D_{m-1,n})$ of data for controlling states of light emission at respective light-emitting regions formed of the scanning electrode in an $(m-1)^{th}$ row from a value $(D_{m,n})$ of data for controlling states of light emission at respective light-emitting regions formed of said scanning electrode in said m^{th} row, is inputted as an input value in said comparator, and said input value, inputted in said comparator, is compared with a first reference value and a second reference value at said comparator;

(1) when said input value is not smaller than said first reference value, said first switching circuit is maintained in an ON state for a predetermined duration shorter than said fixed duration on a basis of an output from said comparator such that during said predetermined duration, a first voltage V_1 is applied to the data electrode in said n^{th} column;

(2) when said input value is not greater than said second reference value, said second switching circuit is maintained in an ON state for a predetermined duration shorter than said fixed duration on a basis of said output from said comparator such that during said predetermined duration, a second voltage V_2 is applied to the data electrode in said n^{th} column; and

(3) when said input value is smaller than said first reference value but is greater than said second reference value, said first switching circuit and said second switching circuit are maintained in OFF-states, respectively.

2. (Original) The fixed pixel display device according to claim 1, wherein, when a difference between a voltage to be applied to said scanning electrode and a voltage to be applied to said data electrode is assumed to be ΔV, said first voltage V_1 is a voltage to be applied to said data electrode to obtain a maximum value of ΔV, and said second voltage V_2 is a voltage to be applied to said data electrode to obtain a minimum value of ΔV.

3. (Original) The fixed pixel display device according to claim 1, wherein said output circuit is a current buffer circuit comprising a CMOS circuit.

4. (Currently amended) A cold cathode field electron emission display device comprising a cathode panel and an anode panel joined together at peripheral edge portions thereof, wherein:

said cathode panel is composed of:

(a) a support,

(b) a multiple number N ($N \geq 2$) of stripe-shaped cathode electrodes formed on said support and extending in a first direction,

(c) an insulating layer formed over said support and cathode electrodes,

(d) another multiple number M ($M \geq 2$) of stripe-shaped gate electrodes formed on said insulating layer and extending in a second direction different from said first direction, and

(e) electron-emitting regions located at overlap regions of said cathode electrodes and said gate electrodes;

said anode panel is composed of a substrate and phosphor regions and an anode electrode formed on said substrate and arranged corresponding to the electron-emitting regions;

said electron-emitting regions are composed of electron-emitting portions located in bottom parts of holes arranged in said gate electrodes and insulating layer;

said cold cathode field electron emission display device is further provided with:

(f) actuation drivers connected to the respective cathode electrodes to actuate said cathode electrodes;

said actuation drivers each comprises a switching circuit, an output circuit, and a subtraction circuit;

said switching circuit is provided with:

(A) a first switching circuit for applying a first voltage V_1 to the corresponding cathode electrode,

(B) a second switching circuit for applying a second voltage V_2 ($V_2 \geq V_1$) to the corresponding cathode electrode, and

(C) a comparator for performing on/off control of said first switching circuit and second switching circuit;

a voltage, outputted from said output circuit on a basis of a value $D_{m,n}$ (m: any one of 2, 3, ..., M; n: 1, 2, ..., N) of data for controlling states of electron emission at a multiple number N of electron-emitting regions formed of an m^{th} gate electrode, is applied for a fixed duration to an n^{th} cathode electrode; and

a value $(D_{m,n} - D_{m-1,n})$, obtained by subtracting at said subtraction circuit a value $D_{m-1,n}$ of data for controlling states of electron emission at the respective electron-emitting regions formed of an $(m-1)^{th}$ gate electrode from a value $D_{m,n}$ of data for

controlling states of electron emission at the respective electron-emitting regions composed by said m^{th} gate electrode, is inputted as an input value in said comparator, and said input value, inputted in said comparator, is compared with a first reference value and a second reference value at said comparator;

(1) when said input value is not smaller than said first reference value, said first switching circuit is maintained in an ON state for a predetermined duration shorter than said fixed duration on a basis of an output from said comparator such that during said predetermined duration, a first voltage V_1 is applied to said n^{th} cathode electrode;

(2) when said input value is not greater than said second reference value, said second switching circuit is maintained in an ON state for a predetermined duration shorter than said fixed duration on a basis of said output from said comparator such that during said predetermined duration, a second voltage V_2 is applied to the n^{th} cathode electrode; and

(3) when said input value is smaller than said first reference value but is greater than said second reference value, said first switching circuit and said second switching circuit are maintained in OFF-states, respectively.

5. (Original) The cold cathode field electron emission display device according to claim 4, wherein, when a difference between a voltage to be applied to said gate electrode and a voltage to be applied to said cathode electrode is assumed to be ΔV_{GC}, said first voltage V_1 is a voltage to be applied to said cathode electrode to obtain a maximum value of ΔV_{GC}, and said second voltage V_2 is a voltage to be applied to said cathode electrode to obtain a minimum value of ΔV_{GC}.

6. (Original) The cold cathode field electron emission display device according to claim 4, wherein said output circuit is a current buffer circuit comprising a CMOS circuit.

7. (Currently amended) A cold cathode field electron emission display device comprising a cathode panel and an anode panel joined together at peripheral edge portions thereof, wherein:

said cathode panel is composed of:

(a) a support,

(b) a multiple number M ($M \geq 2$) of stripe-shaped cathode electrodes formed on said support and extending in a first direction,

(c) an insulating layer formed over said support and cathode electrodes,

(d) another multiple number N ($N \geq 2$) of stripe-shaped gate electrodes formed on said insulating layer and extending in a second direction different from said first direction, and

(e) electron-emitting regions located at overlap regions of said cathode electrodes and said gate electrodes;

said anode panel is composed of a substrate and phosphor regions and an anode electrode formed on said substrate and arranged corresponding to the electron-emitting regions;

said electron-emitting regions are composed of electron-emitting portions located in bottom parts of holes arranged in said gate electrodes and insulating layer;

said cold cathode field electron emission display device is further provided with:

(f) actuation drivers connected to the respective gate electrodes to actuate said gate electrodes;

said actuation drivers each comprises a switching circuit, an output circuit, and a subtraction circuit;

said switching circuit is provided with:

(A) a first switching circuit for applying a first voltage V_1 to the corresponding gate electrode,

(B) a second switching circuit for applying a second voltage V_2 ($V_2 < V_1$) on the corresponding gate electrode, and

(C) a comparator for performing on/off control of said first switching circuit and second switching circuit;

a voltage, outputted from said output circuit on a basis of a value $D_{m,n}$ (m: any one of 2, 3, ..., M; n: 1, 2, ..., N) of data for controlling states of electron emission at a multiple number N of electron-emitting regions formed of an m^{th} cathode electrode, is applied for a fixed duration to an n^{th} gate electrode; and

a value $(D_{m,n} - D_{m-1,n})$, obtained by subtracting at said subtraction circuit a value $D_{m-1,n}$ of data for controlling states of electron emission at the respective light-emitting regions formed of an $(m-1)^{th}$ cathode electrode from a value $D_{m,n}$ of data for controlling states of electron emission at the respective electron-emitting regions composed by said m^{th} cathode electrode, is inputted as an input value in said comparator, and said input value, inputted in said comparator, is compared with a first reference value and a second reference value at said comparator;

(1) when said input value is not smaller than said first reference value, said first switching circuit is maintained in an ON state for a predetermined duration shorter than said fixed duration on a basis of an output from said comparator such that

during said predetermined duration, a first voltage V_1 is applied to said n^{th} gate electrode;

(2) when said input value is not greater than said second reference value, said second switching circuit is maintained in an ON state for a predetermined duration shorter than said fixed duration on a basis of said output from said comparator such that during said predetermined duration, a second voltage V_2 is applied to the n^{th} gate electrode; and

(3) when said input value is smaller than said first reference value but is greater than said second reference value, said first switching circuit and said second switching circuit are maintained in OFF-states, respectively.

8. (Original) The cold cathode field electron emission display device according to claim 7, wherein, when a difference between a voltage to be applied to said gate electrode and a voltage to be applied to said cathode electrode is assumed to be ΔV_{GC}, said first voltage V_1 is a voltage to be applied to said gate electrode to obtain a maximum value of ΔV_{GC}, and said second voltage V_2 is a voltage to be applied to said gate electrode to obtain a minimum value of ΔV_{GC}.

9. (Original) The cold cathode field electron emission display device according to claim 7, wherein said output circuit is a current buffer circuit comprising a CMOS circuit.